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you can free download Biometrical Techniques In Plant Breeding book pdf on ManyBooks.org library. Has since 1991, it is one of the popular books all over the world.The present invention relates to a semiconductor device and its manufacturing method, and more particularly to a technique which is effectively applied to a semiconductor device having a multilayer interconnection structure in which interconnections are connected through vias formed in an interlayer insulating film and to a manufacturing method thereof. In accordance with miniaturization of semiconductor elements, the area occupied by the semiconductor elements has been decreased. Along with this, the area occupied by the interconnections within the semiconductor elements has been significantly reduced. Along with this, the aspect ratio of vias formed on a semiconductor substrate has been increased, and when forming the vias, air gaps between the interconnections or inner surfaces of contact holes are collapsed. Especially, with the development of the photolithography technique in recent years, the line width of the interconnections has been decreased. Along with this, as the aspect ratio of the contact holes is increased, the fineness of the interconnections is increased, and air gaps between the interconnections or inner surfaces of the contact holes are liable to collapse. Further, the development of the manufacturing techniques and the miniaturization of the semiconductor elements have advanced, and it is necessary to connect the multilayer interconnections through vias of high aspect ratio formed in an interlayer insulating film. However, even when using the above-described techniques, it is difficult to form interconnections having a fine line width in high aspect ratio vias. A technique is proposed in Japanese Unexamined Patent Publication No. 11(1999)-150514 (Patent Document 1) in order to solve the above-described problem. FIG. 5 is a cross-sectional view of a semiconductor device which is proposed in Patent Document 1. In FIG. 5, an interlayer insulating film 102 is formed on a semiconductor substrate 101, and through holes 103 are formed in the interlayer insulating film 102. Then, a barrier metal film 104 is formed on the inner wall surfaces of the through holes 103, and a metal film 105 such as tungsten is filled in the through holes 103 by CVD method, thereby forming the interconnection 106. The interconnection 106 is covered with a CVD oxide film 107, and the CVD oxide film 107 is 6d1f23a050